Growth and Engineering of High Aspect-Ratio AAO Templates Integrated on Silicon Substrates

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ABSTRACT

Scientists at Enable IPC Corporation have developed a complementary metal oxide semiconductor (CMOS) compatible process for growing and patterning high aspect-ratio anodized aluminum oxide (AAO) templates integrated on silicon (Si) substrates that can be used for the fabrication of vertical arrays of nanowires having high surface area. Honeycomb-shaped, ordered arrays of aluminum nanopore templates with uniform-size cylindrical pores can be produced utilizing an anodization process along with a subsequent pore-widening processes carried out at an elevated temperature. Enable IPC is developing a microbattery utilizing this technology to improve cathode performance.

Keywords: anodized aluminum oxide, nanowire, high surface area, nanopore templates, pore-widening process.

1 INTRODUCTION

The use of nanowire cathodes has been researched by several organizations, including Boundless Corporation [1] and the Jet Propulsion Laboratory [2]. The evidence from this research suggests that nanowire-structured cathodes can provide greater power density due primarily to the increase in surface area. However, the actual structuring of these nanowires for CMOS compatibility involves a number of time consuming tasks. Enable IPC has successfully manufactured nanowires directly on silicon substrates, eliminating some of these steps.

A chip-scale Lithium (Li)-ion rechargeable microbattery having high power and capacity can be realized by fabricating nanowire-based cathodes on silicon (Si) substrates. These nanowire cathodes provide greater surface area, thus enhancing power. In order to grow a vertical array of nanowires with a high aspect-ratio, one must create a suitable nanopore template. Ordered arrays of alumina nanopore templates with uniform-size cylindrical pores can be made by utilizing an anodization process along with a subsequent pore-widening processes carried out at an elevated temperature. Advantages of our process over conventional processes for anodized aluminum oxide (AAO) fabrication include: 1) The aspect-ratio of the cylindrical nanopores in our templates are over 400:1, and thus enable the growth of the same aspect-ratio nanowires, which result in greatly increased surface area; 2) Our process can be used for the direct growth of a thick AAO template on Si substrates; 3) A significant level of control over the patterning of an AAO template and, therefore, the positioning of nanowires is possible; and 4) A great degree of control over the thickness of an AAO template, and therefore, the height of the nanowires, is also possible.

2 EXPERIMENTAL RESULTS

A CMOS compatible process for growing and patterning high aspect-ratio AAO templates integrated on Si substrates has been developed for the fabrication of a vertical array of nanowires having high surface area. Straight, ordered pores with diameters of 10-200 nm can be made with ultra high-density pore structures (10^{10} to 10^{12} cm^{-2}).

Anodized alumina has proven to be a key material in fabricating these structures. Unlike track-etched membranes, anodized alumina pores have little or no tilt with respect to the surface, resulting in an isolated, non-connecting pore structure. Anodized alumina is electrically insulating (10^{18} ohm-cm), optically transparent over a wide energy band range, chemically stable, and compatible with CMOS processes. Aluminum anodization in oxalic or sulfuric acid resulting in highly ordered honeycomb structures has been previously reported [3].

Pore dimensions of 10 nm to 200 nm can be controlled by adjusting the anodizing solution composition and applied current density. Experiments at Enable IPC have shown that pore dimensions and the distance between pores (pore density) in alumina templates can be controlled by selecting specific anodizing solutions, potential, current density, temperature and agitation. We have successfully made pores as small as 10 nm with porosity on the order of 30-40%.

We are able to promote greater control over the patterning of the nanopore arrays by utilizing a two-step anodization process. The first anodized layer is removed, and acts as the nucleation site for a second anodization, which promotes highly ordered pore growth. After each anodization is completed, a subsequent pore-widening process, using 5% H_3PO_4 at an elevated temperature (about 80°C), follows. Elevating the temperature is thought to help connect cylindrical pores in the bottom layer to the top layer of the AAO template. A cross-sectional view of a field emission scanning electron microscope (FESEM) image of the AAO template consisting of cylindrical pores of 50 nm in diameter is shown in Figure 1. The fabrication sequence to create a patterned AAO template with high

aspect-ratio cylindrical pores consists of the steps listed below, and is illustrated in Figure 2.

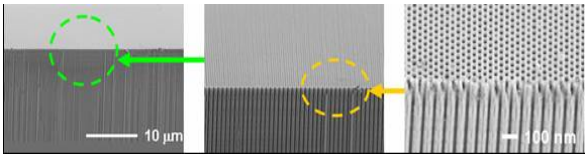

Figure 1: FESEM micrographs of a high aspect-ratio (400:1) AAO template grown on a silicon substrate (pore diameter is about 50nm).

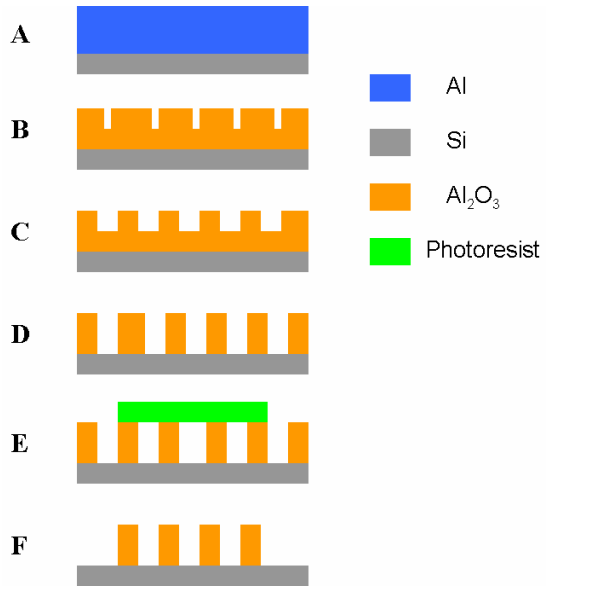

Figure 2: Fabrication of a patterned high aspect-ratio AAO template pre-grown on a Si substrate.

(A) 20μm thick Aluminum (Al) is sputtered on a Si substrate. (B) Anodization with 0.1M Oxalic acid is performed at a constant voltage. This process initiates the growth of cylindrical pores from the surface of the Al film. (C) Etching with chromic acid is performed. This process polishes the inner surface of cylindrical pores. (D) Another anodization is performed to enhance the continuous growth of cylindrical pores in the template. (E) An optical lithography step is performed to define 10μm wide photoresist patterns on the surface of the AAO template. (F) Finally, ion-milling is performed to transfer the photoresist pattern onto the AAO template.

Figure 3 shows FESEM micrographs of an AAO pattern. The word pattern ("IP") was generated by optical lithography and a subsequent ion-milling process after the growth of a high aspect-ratio AAO template. This letter pattern was grown directly on a Si substrate and a subsequent ion-milling process used to pattern the AAO template [4].

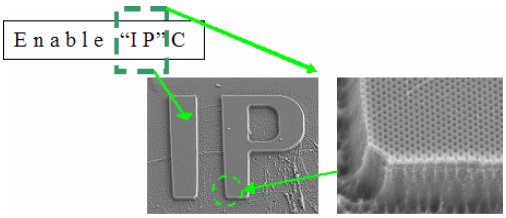

Figure 3: FESEM micrographs of the letter patterns of "IP"(in Enable IPC) in a nanopore template (left). The width of the letters is about 10 μm. The diameter of nanopores (right) is about 50 nm.

The nanopores of a high aspect-ratio AAO template are filled with cathode materials for Li-ion rechargeable batteries. The template is then etched away leaving free-standing nanowires of cathode materials, providing greater surface area, and thus the potential for higher capacities and charge/discharge rates. Using this technology, we are developing processes for integrating these nanowires as cathodes with actual micro-battery materials [5].

3 CONCLUSIONS

We have developed a novel anodization process which can produce nanopore templates with high aspect-ratios (400:1) and ordered nanopore arrays. The diameter and length of the nanowires can be precisely controlled and optimized to increase their surface area. Using this process to create nanowire cathode materials has the potential to significantly increase the effective cathode surface area of microbatteries.

4 ACKNOWLEDGEMENTS

This work was done by Enable IPC Corporation under its in house research and development program for developing nanowire-based lithium-ion rechargeable batteries.

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